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UNITRODE

UCC1946
UCC2946
UCC3946

Microprocessor Supervisor with Watchdog Timer

FEATURES

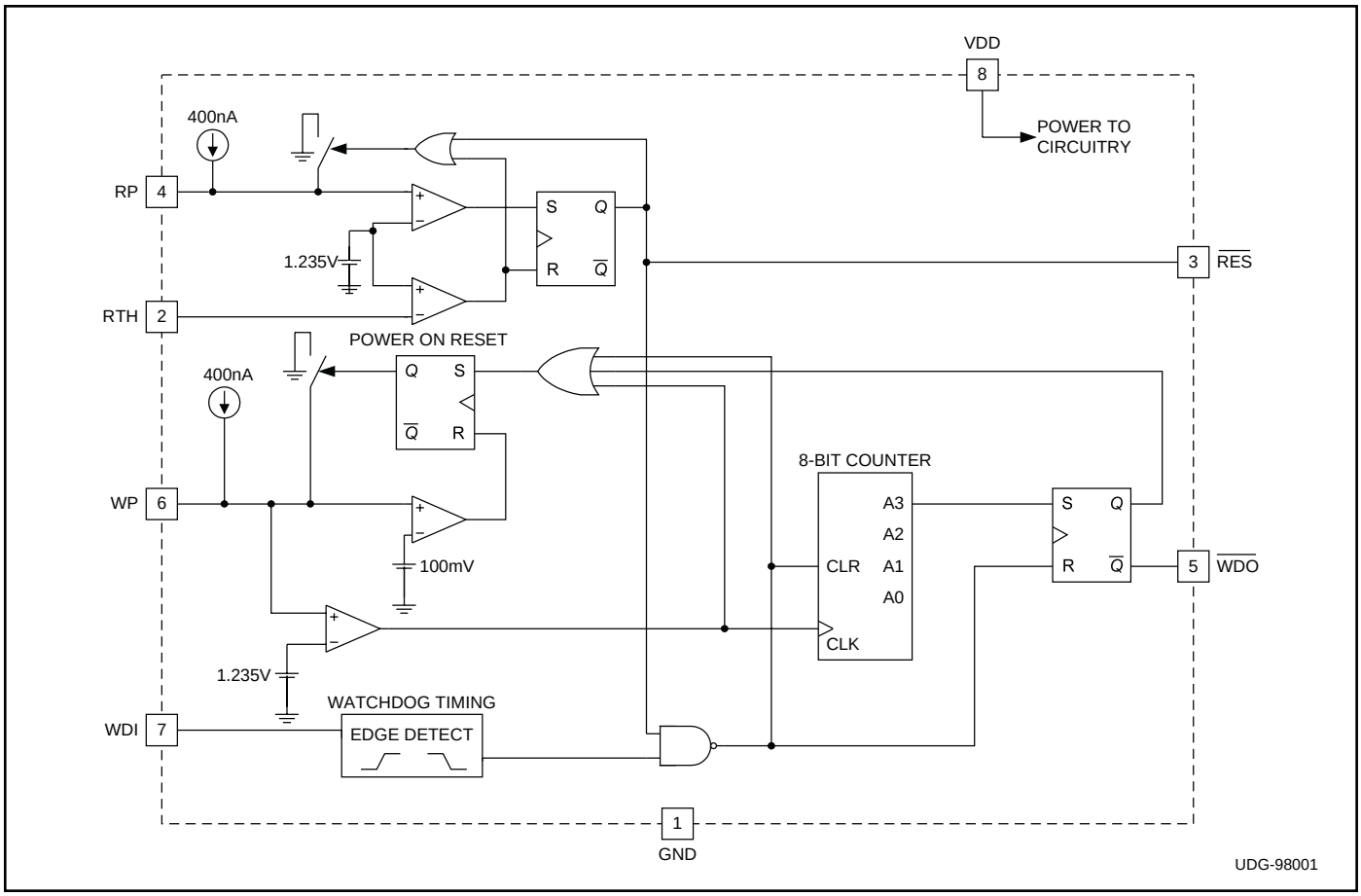
- Fully Programmable Reset Threshold
- Fully Programmable Reset Period
- Fully Programmable Watchdog Period
- 2% Accurate Reset Threshold
- VDD Can Go as Low as 2V
- 18µA Maximum IDD
- Reset Valid Down to 1V

DESCRIPTION

The UCC3946 is designed to provide accurate microprocessor supervision, including reset and watchdog functions. During power up, the IC asserts a reset signal $\overline{RES}$ with VDD as low as 1V. The reset signal remains asserted until the VDD voltage rises and remains above the reset threshold for the reset period. Both reset threshold and reset period are programmable by the user. The IC is also resistant to glitches on the VDD line. Once $\overline{RES}$ has been deasserted, any drops below the threshold voltage need to be of certain time duration and voltage magnitude to generate a reset signal. These values are shown in Figure 1. An I/O line of the microprocessor may be tied to the watchdog input (WDI) for watchdog functions. If the I/O line is not toggled within a set watchdog period, programmable by the user, $\overline{WDO}$ will be asserted. The watchdog function will be disabled during reset conditions.

The UCC3946 is available in 8-pin SOIC(D), 8-pin DIP (N or J) and 8-pin TSSOP(PW) packages to optimize board space.

BLOCK DIAGRAM



Note: Pinout represents the 8-pin TSSOP package.

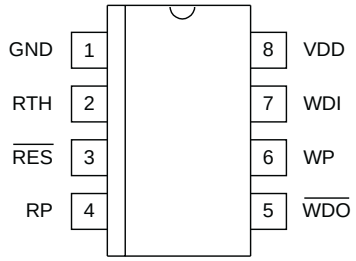
ABSOLUTE MAXIMUM RATINGS

V_{IN} 10V
Storage Temperature . . . . . –65°C to +150°C
Junction Temperature . . . . . –55°C to +150°C
Lead Temperature (Soldering, 10 sec.) . . . . . +300°C

Currents are positive into, negative out of the specified terminal. Consult Packaging Section of the Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAM

SOIC-8, TSSOP-8, DIL-8 (Top View)
D, PW, N or J Package



ELECTRICAL CHARACTERISTICS: Unless otherwise specified, VDD = 2.1V to 5.5V for UCC1946 and UCC2946; VDD = 2V to 5.5V for UCC3946; TA = 0°C to 70°C for UCC3946, –40°C to 95°C for UCC2946, and –55°C to 125°C for UCC1946; $T_A = T_J$

PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
		UCC3946			UCC1946 & UCC2946			
Operating Voltage		2.0		5.5	2.1		5.5	V
Supply Current			10	18		12	18	µA
Minimum VDD	(Note 1)			1			1.1	V
Reset Section								
Reset Threshold	VDD Rising	1.210	1.235	1.260	1.170	1.235	1.260	V
Threshold Hysteresis			15			15		mV
Input Leakage				5			5	nA
Output High Voltage	I_{SOURCE} = 2mA	V_{DD} – 0.3			V_{DD} – 0.3			V
Output Low Voltage	I_{SINK} = 2mA			0.1			0.1	V
	VDD = 1V, I_{SINK} = 20uA			0.2			0.4	V
VDD to Output Delay	VDD = -1mV/µs (Note 2)		120			120		µs
Reset Period	C_{RP} = 64nF	160	200	260	140	200	320	ms
Watchdog Section								
WDI Input High		0.7· V_{DD}			0.7· V_{DD}			V
WDI Input Low				0.3· V_{DD}			0.3· V_{DD}	V
Watchdog Period	C_{WP} = 64nF	1.12	1.60	2.08	0.96	1.60	2.56	s
Watchdog Pulse Width		50			50			ns
Output High Voltage	I_{SOURCE} = 2mA	V_{DD} – 0.3			V_{DD} – 0.3			V
Output Low Voltage	I_{SINK} = 2mA			0.1			0.1	V

Note 1: This is the minimum supply voltage where $\overline{RES}$ is considered valid.
Note 2: Guaranteed by design. Not 100% tested in production.

PIN DESCRIPTIONS

GND: Ground reference for the IC.

$\overline{\text{RES}}$: This pin is high only if the voltage on the RTH has risen above 1.235V. Once RTH rises above the threshold, this pin remains low for the reset period. This pin will also go low and remain low if the RTH voltage dips below 1.235V for an amount of time determined by Figure 1.

RTH: This input compares its voltage to an internal 1.25V reference. By using external resistors, a user can program any reset threshold he wishes to achieve.

RP: This pin allows the user to program the reset period by adjusting an external capacitor.

VDD: Supply voltage for the IC.

WDI: This pin is the input to the watchdog timer. If this pin is not toggled or strobed within the watchdog period, $\overline{\text{WDO}}$ is asserted.

$\overline{\text{WDO}}$: This pin is the watchdog output. This pin will be asserted low if the WDI pin is not strobed or toggled within the watchdog period.

WP: This pin allows the user to program the watchdog period by adjusting an external capacitor.

APPLICATION INFORMATION

The UCC3946 supervisory circuit provides accurate reset and watchdog functions for a variety of microprocessor applications. The reset circuit prevents the microprocessor from executing code during undervoltage conditions, typically during power-up and power-down. In order to prevent erratic operation in the presence of noise, voltage “glitches” whose voltage amplitude and time duration are less than the values specified in Fig. 1 are ignored.

The watchdog circuit monitors the microprocessor’s activity, if the microprocessor does not toggle WDI during the programmable watchdog period $\overline{\text{WDO}}$ will go low, alerting the microprocessor’s interrupt of a fault. The $\overline{\text{WDO}}$ pin is typically connected to the non-maskable input of the microprocessor so that an error recovery routine can be executed.

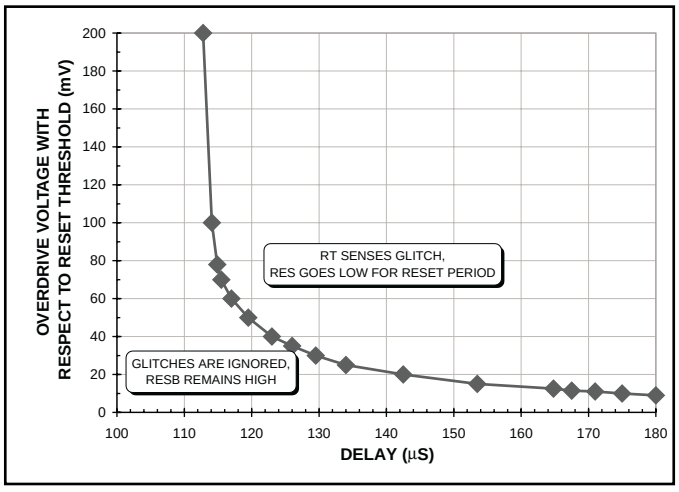


Figure 1. Overdrive voltage vs. delay to output low on RESB.

Slew rate: –1V/mS; monitored voltage = V_{DD}.

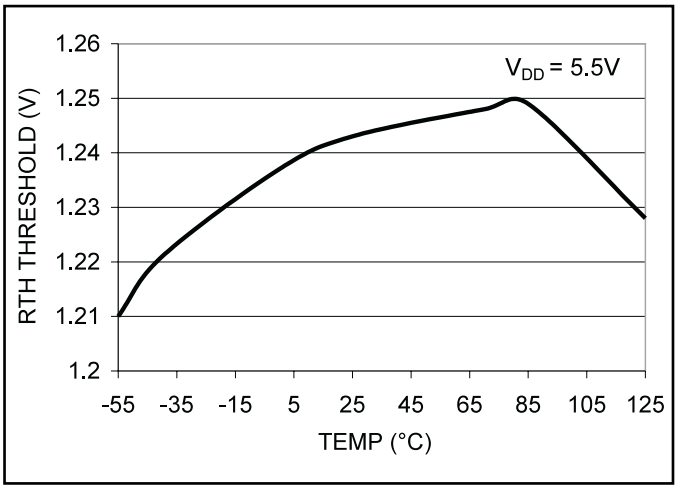


Figure 2. Typical RTH threshold vs. temperature.

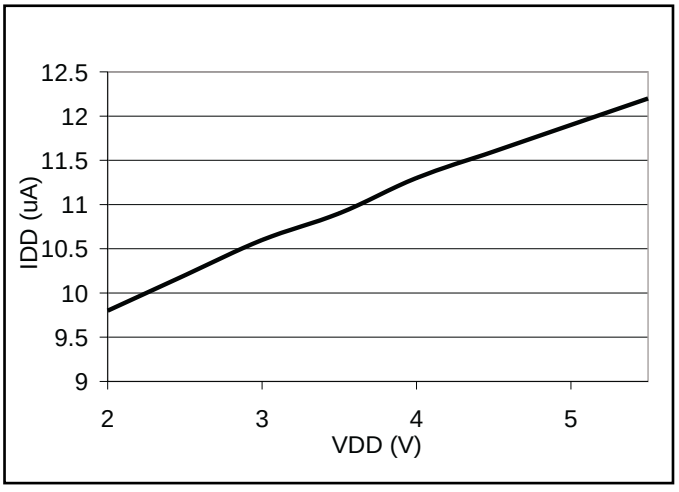
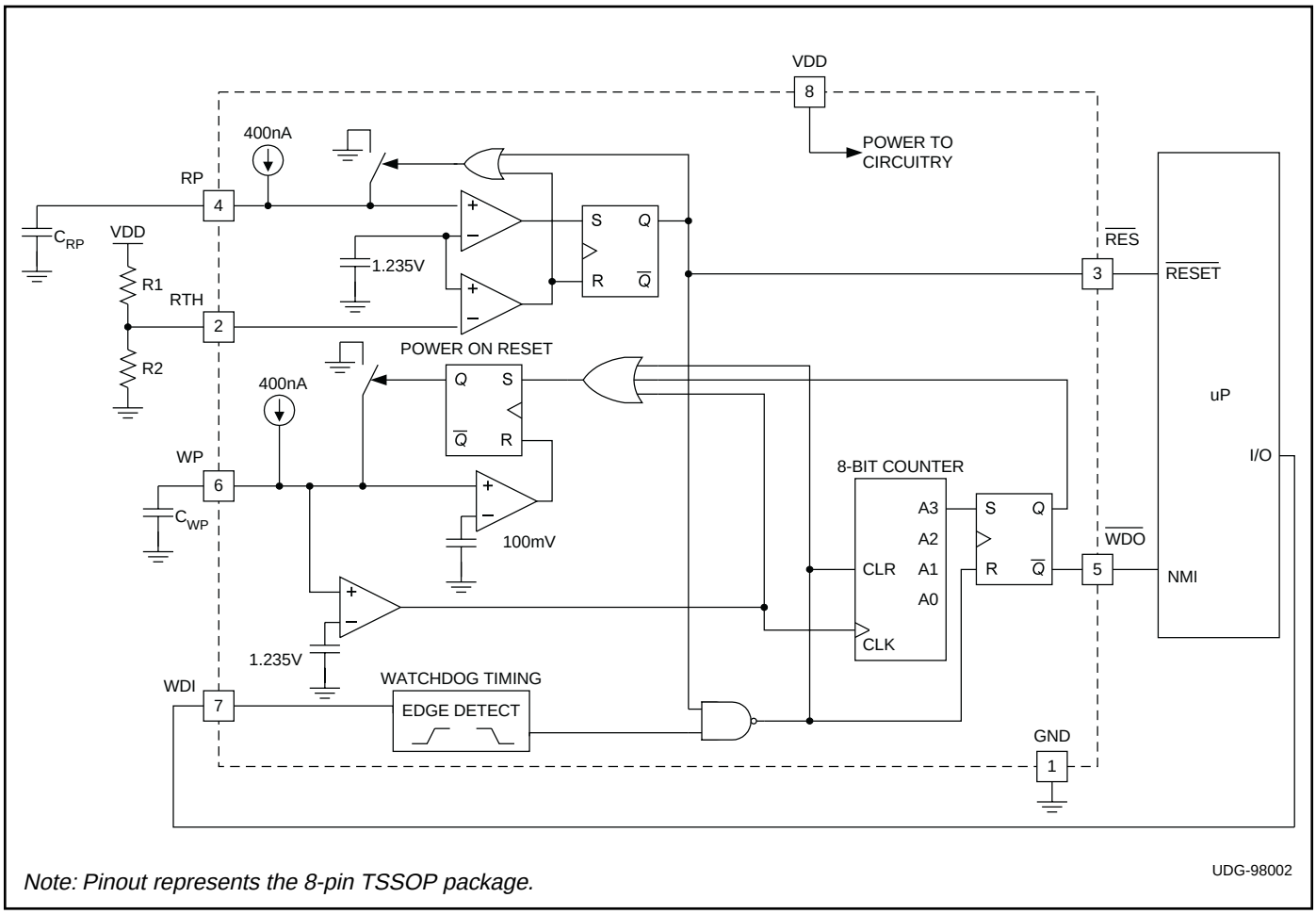


Figure 3. Typical IDD vs VDD.

APPLICATION INFORMATION (cont.)



Note: Pinout represents the 8-pin TSSOP package.

Figure 4. Typical application diagram.

Programming the Reset Voltage and Reset Period

The UCC3946 allows the reset trip voltage to be programmed with two external resistors. In most applications VDD is monitored by the reset circuit, however, the design allows voltages other than VDD to be monitored. Referring to Fig. 4, the voltage below which reset will be asserted is determined by:

$$V_{RESET} = 1.235 \bullet \frac{R1 + R2}{R2}$$

In order to keep quiescent currents low, resistor values in the megaohm range can be used for R1 and R2. A manual reset can be easily implemented by connecting a momentary push switch in parallel with R2. $\overline{RES}$ is guaranteed to be low with VDD voltages as low as 1V.

Once VDD rises above the programmed threshold, $\overline{RES}$ remains low for the reset period defined by:

$$T_{RP} = 3.125 \bullet C_{RP}$$

where T_{RP} is time in milliseconds and C_{RP} is capacitance in nanofarads. C_{RP} is charged with a precision current source of 400nA, a high quality, low leakage capacitor (such as an NPO ceramic) should be used to maintain timing tolerances. Fig. 5 illustrates the voltage levels and timings associated with the reset circuit.

Programming the Watchdog Period

The watchdog period is programmed with C_{WP} as follows:

$$T_{WP} = 25 \bullet C_{WP}$$

where T_{WP} is in milliseconds and C_{WP} is in nanofarads. A high quality, low leakage capacitor should be used for C_{WP}. The watchdog input WDI must be toggled with a high/low or low/high transition within the watchdog period to prevent $\overline{WDO}$ from assuming a logic level low. $\overline{WDO}$ will maintain the low logic level until WDI is toggled or $\overline{RES}$ is asserted. If at any time $\overline{RES}$ is asserted, $\overline{WDO}$ will assume a high logic state and the watchdog period will be reinitiated. Fig. 6 illustrates the timings associated with the watchdog circuit.

APPLICATION INFORMATION (cont.)

Connecting $\overline{WDO}$ to $\overline{RES}$

In order to provide design flexibility, the reset and watchdog circuits in the UCC3946 have separate outputs. Each output will independently drive high or low, depending on circuit conditions explained previously.

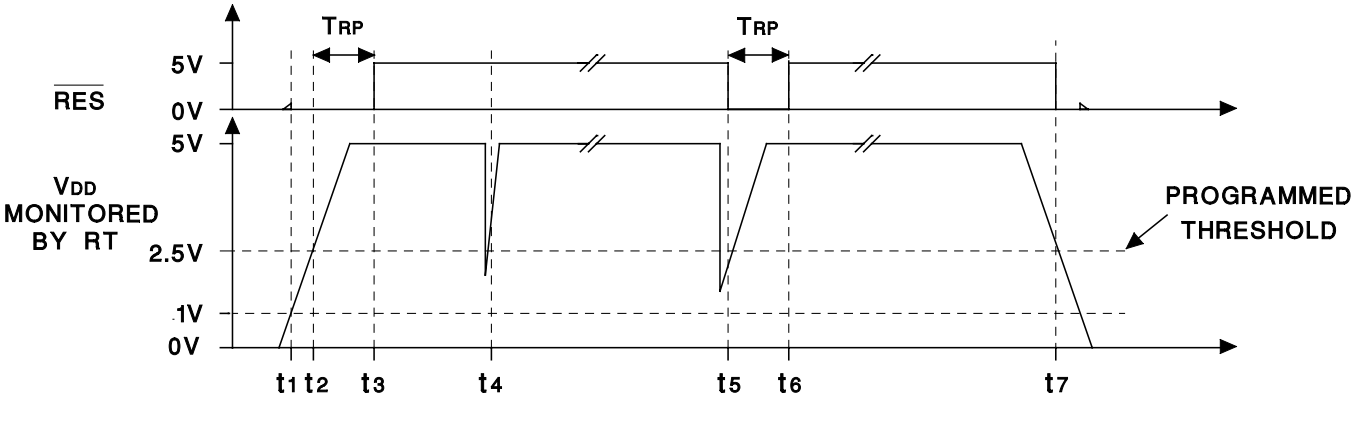
In some applications, it may be desirable for either the $\overline{RES}$ or $\overline{WDO}$ to reset the microprocessor. This can be done by connecting $\overline{WDO}$ to $\overline{RES}$. If the pins try to drive to different output levels, the low output level will dominate. Additional current will flow from VDD to GND during these states. If the application cannot support additional current (during fault conditions), $\overline{RES}$ and $\overline{WDO}$ can be connected to the inputs of an OR gate whose output is connected to the microprocessor's reset pin.

Layout Considerations

A 0.1µF capacitor connected from V_{DD} to GND is recommended to decouple the UCC3946 from switching transients on the V_{DD} supply rail.

Since RP and WP are precision current sources, capacitors C_{RP} and C_{WP} should be connected to these pins with minimal trace length to reduce board capacitance. Care should be taken to route any traces with high voltage potential or high speed digital signals away from these capacitors.

Resistors R1 and R2 generally have a high ohmic value, traces associated with these parts should be kept short in order to prevent any transient producing signals from coupling into the high impedance RTH pin.



t1: V_{DD} > 1V, $\overline{RES}$ is guaranteed low.

t2: V_{DD} > programmed threshold, $\overline{RES}$ remains low for T_{RP}.

t3: T_{RP} expires, $\overline{RES}$ pulls high.

t4: Voltage glitch occurs, but is filtered at the RTH pin, $\overline{RES}$ remains high.

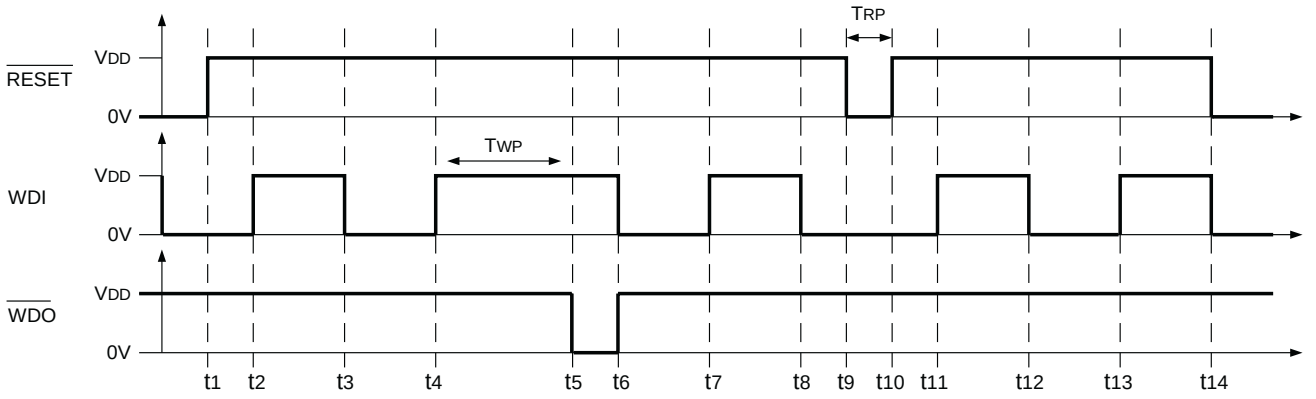
t5: Voltage glitch occurs whose magnitude and duration is greater than the RTH filter, $\overline{RES}$ is asserted for T_{RP}.

t6: On completion of the T_{RP} pulse the R_{TH} voltage has returned and $\overline{RES}$ is pulled high.

t7: V_{DD} dips below threshold (minus hysteresis), $\overline{RES}$ is asserted.

Figure 5. Reset circuit timings.

APPLICATION INFORMATION (cont.)



t1: Microprocessor is reset.

t2: WDI is toggled some time after reset, but before T_{WP} expires.

t3: WDI is toggled before T_{WP} expires.

t4: WDI is toggled before T_{WP} expires.

t5: WDI is not toggled before T_{WP} expires and $\overline{WDO}$ asserts low, triggering the microprocessor to enter an error recovery routine.

t6: The microprocessor's error recovery routine is executed and WDI is toggled, reinitiating the watchdog timer.

t7: WDI is toggled before T_{WP} expires.

t8: WDI is toggled before T_{WP} expires.

t9: $\overline{RES}$ is momentarily triggered, $\overline{RES}$ is asserted low for T_{RP}.

t10: Microprocessor is reset, $\overline{RES}$ pulls high.

t11: WDI is toggled some time after reset, but before T_{WP} expires.

t12: WDI is toggled before T_{WP} expires.

t13: WDI is toggled before T_{WP} expires.

t14: V_{DD} dips below the reset threshold, $\overline{RES}$ is asserted.

Figure 6. Watchdog circuit timings.

UNITRODE CORPORATION
7 CONTINENTAL BLVD. • MERRIMACK, NH 03054
TEL. (603) 424-2410 • FAX (603) 424-3460